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**UNITED STATES PATENT APPLICATION**

**FOR**

**A METHOD AND APPARATUS FOR ANALOG  
COMPENSATION OF DRIVER OUTPUT  
SIGNAL SLEW RATE AGAINST DEVICE  
IMPEDANCE VARIATION**

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COMPENSATION OF DRIVER OUTPUT  
SIGNAL SLEW RATE AGAINST DEVICE  
IMPEDANCE VARIATION**

**RELATED APPLICATIONS**

**[001]** This application is a continuation of U.S. Application No. 10/348,878, filed January 21, 2003, currently pending, which is a divisional of U.S. Patent No. 6,571,376, issued May 27, 2003.

**FIELD OF THE INVENTION**

**[002]** One or more embodiments relate generally to an output driver. One embodiment relates to an apparatus and method for analog compensation of driver output signal slew rate against device impedance variation.

**BACKGROUND OF THE INVENTION**

**[003]** High speed I/O (input/output) buffers can improve transmitted and received signal quality through the use of on-chip signal termination. One technique that is often used to provide on-chip signal termination is the formation of an Nwell resistor structure as the die termination. Nwell material is often selected due to its highly resistive structure. In addition to being highly resistive, an Nwell structure is simple to create and consumes a relatively small die area compared to, for example a polyresistor.

**[004]** Unfortunately, Nwell material and Nwell resistive elements created using such material are prone to wide variations in resistivity. In fact, materials and processing used to create resistive elements using Nwell material are subject to wide variations. Therefore, without some sort of external compensation, the resistance of the termination device can easily vary by 300%. Consequently, because output signals are driven through such on-chip resistive termination, the effect of the resistance variation on an output signal slew rate can be significant. Therefore compensation is required to regulate the output driver slew rate according to the strength of the on-chip termination resistor.

**[005]** As a result, most sensitive high speed output drivers use external compensation to maintain correct functionality across the wide resistive range of the Nwell on-chip termination resistor. Such conventional techniques often utilize a digital approach, which directs the activation and de-activation of various buffers to regulate the output drivers. As such, digital regulation of the output drivers is required to compensate for the variations in the on-chip resistive termination. Usually, this is performed using a digital compensation block requiring extra pins at higher manufacturing costs.

**[006]** Accordingly, compensation circuits, particularly ones which employ a digital approach, have historically been trouble spots, due to their complexity, the need for calibration and their potential to interfere with normal buffer operation. In other words,

circuit designers are required to provide some sort of compensation mechanism for interfacing with legacy drivers to meet timing specifications. Moreover, such compensation mechanisms are required due to the fact that signals subject to inadequate/excessive on-chip termination will incur signaling integrity problems.

**[007]** As such, signals driven through excessive on-chip termination will incur substantial delays in completing falling/rising signal transition. As a result, the system will incur timing problems, such as violation of set-up time at signal receivers due to the delay in rising/falling signal transition. Conversely, when the on-chip termination resistance is too small, uncontrolled fast signaling of output signal slew rates will result. As a result, this uncontrolled fast switching creates potential signal integrity problems and signal corruption due to reflection. Moreover, electromagnetic interference is aggravated when uncontrolled fast switching of output signals results. Therefore, there remains a need to overcome one or more of the limitations in the above-described, existing art.

BRIEF DESCRIPTION OF THE DRAWINGS

**[008]** The features, aspects, and advantages of the present invention will become more fully apparent from the following Detailed Description and appended claims when taken in conjunction with accompanying drawings in which:

**[009]** FIG. 1 depicts a block diagram illustrating a conventional output driver as known in the art.

**[0010]** FIGS. 2A-2E depict timing diagrams illustrating pre-drive signals resulting in a driver output signal at the pad of the output driver, as depicted in FIG. 1.

**[0011]** FIG. 3 depicts a block diagram illustrating a crowbar current within the conventional output driver as depicted in FIG. 1.

**[0012]** FIGS. 4A and 4B depict timing diagrams illustrating pre-drive signals resulting in a crowbar current within the output driver, as depicted in FIG. 3.

**[0013]** FIG. 5 depicts a block diagram illustrating an output driver utilizing analog compensation of output driver signal slew rate against device impedance variation in accordance with one embodiment.

**[0014]** FIG. 6 depicts a block diagram illustrating the driver, as depicted in FIG. 1, during a falling signal transition in accordance with a further embodiment.

**[0015]** FIGS. 7A-7C depict timing diagrams illustrating analog compensation of a driver output signal slew rate against device impedance variation in accordance with one embodiment.

**[0016]** FIG. 8 depicts a block diagram illustrating a system chipset utilizing a driver, as depicted in FIGS. 5 and 6, in accordance with a further embodiment.

**[0017]** FIG. 9 depicts a block diagram illustrating an electronic system utilizing a driver, as depicted in FIGS. 5 and 6, in accordance with a further embodiment.

DETAILED DESCRIPTION

**[0018]** A method and apparatus for analog compensation of driver output signal slew rate against termination device impedance variation are described. In one embodiment, the embodiments described herein describe an output driver. The output driver includes a signal termination device coupled to a driver output pad. In one embodiment, the driver includes a pull-up circuit having at least one pull-up device coupled between a driver supply voltage and the signal termination device. The driver also includes a pull-up circuit having at least one pull-down device coupled between a driver ground and the signal termination device. In one embodiment, the pull-up circuit includes a pull-up compensation resistive element and the pull-down circuit includes a pull-down compensation resistive element. Accordingly, the pull-up and pull-down compensation resistive elements provide analog compensation of output driver signal slew rate against driver impedance variation. In one embodiment, a slew rate of the driver output signal is within a predetermined slew rate range to avoid uncontrolled fast switching in the driver output signal as well as unnecessarily slow switching of the driver output signal.

**[0019]** In the following description, for the purposes of explanation, numerous specific details are set forth to provide a thorough understanding of the embodiments described herein. It will be apparent, however, to one skilled in the art that the embodiments described herein may be practiced without some of these specific details. For example, various signals, layout patterns, memory cell configurations and circuits, and logic circuits may be modified according to the embodiments described herein.

**[0020]** In addition, the following description provides examples, and the accompanying drawings show various examples for the purposes of illustration. However, these examples should not be construed in a limiting sense as they are merely intended to provide examples of the embodiments described herein rather than to provide an exhaustive list of all possible implementations of the embodiments described herein. In other instances, well-known structures and devices are shown in block diagram form to avoid obscuring the details of the embodiments described herein.

System Architecture

**[0021]** Referring now to FIG. 1, FIG. 1 depicts a conventional output driver 100, such as an input/output (I/O) driver. As depicted, the driver 100 includes a pair of pull-up devices (110 and 120) and a pair of opposed pull-down devices (130 and 140). However, as described above, output driver 100 includes a signal termination device, which is depicted as utilizing an Nwell termination resistor 150. As described above, the Nwell termination resistor is susceptible to substantial variations (device impedance variation) in resistance once fabricated on a die. In fact, device impedance variations of the termination device can vary by as much as 300%.

**[0022]** The conventional output driver 100 also includes a pull-up pre-driver 180 and a pull-down pre-driver 190. The pull-up pre-driver 180 directs pull-up signals

(PDRVG1) 112 and (PDRVG0) 122. As will be illustrated with reference to FIGS. 2A-2C, the pull-up driver activates the PDRVG1 signal 112, as well as the PDRVG0 signal 122 to cause a rising signal transition at the driver output pad 160. Conversely, to generate a falling signal transition at the output buffer pad 160, the driver 100 includes a pull-down pre-driver 190. The pull-down pre-driver 190 activates a pair of signals (NDRVG1 132 and NDRVG0 142), which when activated drop the voltage level at the driver output pad to achieve a falling signal transition.

**[0023]** However, due to the fact that the output driver 100 utilizes an Nwell termination resistor 150 for signal termination, variations of Nwell termination resistor 150 will affect a slew rate of the driver output signal at the output pad 160. For instance, if the fabricated Nwell termination resistor 150 is generated having an excessive resistance value, the amount of current 170/172 that can be provided to driver output pad 160 during a rising signal transition or pulled from the driver output pad 160 during a falling signal transition will be very slow. As a result, the amount of time required for completion of a falling signal transition or a rising signal transition will be slow, which can lead to problems in meeting timing specifications, such as set-up time of various devices that may be connected to the driver.

**[0024]** Referring now to FIGS. 2A-2E, FIG. 2A illustrates activation of the pull-down signals NDRVG0 132 and NDRVG1 142 during a rising signal transition at the output pad 160. As illustrated, to generate a rising signal transition at the output pad 160 of the driver 100 as depicted in FIG. 1, the pull-down devices 130 and 140 are de-activated by lowering the gate voltage level to a predetermined level. Once the pull-down devices 138 and 140 are turned off, the pull-up devices 110 and 120 are turned on, as illustrated in FIG. 2B, by dropping the voltage level to a predetermined value. However, in the embodiment depicted, pull-up leg 120 is considered the weaker of the pull-up legs and is activated prior to activation of pull-up leg 110.

**[0025]** As such, referring to FIG. 2C, FIG. 2C illustrates optimal output driver signal slew rates due to absence of device impedance variation in the termination resistance. As illustrated, the rising signal transition at the output pad 160 is initially slow while the weak pull-up leg 120 is turned on. However, once both pull-up legs 110 and 120 are turned on, the driver 100 drives high at a greater slew rate due to activation of the strongest pull-up leg 120. As illustrated by FIG. 2C, the driver output pad signal slew rate is within a desired slew rate range due to an absence of signal termination device impedance variation.

**[0026]** Referring again to FIG. 2A, to generate a falling signal transition, pull-up legs 110 and 120 are turned off, as illustrated by FIG. 2B, by the pull-up signals PDRVG0 122 and PDRVG1 112. However, the weaker of the pull-down legs 140 is activated prior to activation of the stronger pull-down leg 130. As illustrated in FIG. 2C, while the pull-down leg 140 begins the falling signal transition, the signal transitions at a slower rate.

However, once both pull-down legs 130 and 140 are activated, the rising signal transition occurs, such that a slew rate of the output signal is within a predetermined slew rate range. Unfortunately, due to the fact that output driver 100 (FIG. 1) utilizes an Nwell resistor as a signal termination device 150, variations of the Nwell termination resistor 150 will affect the slew rate of the driver output signal at the output pad 160, as illustrated with reference to FIGS. 2D and 2E.

**[0027]** Referring to FIG. 2D, FIG. 2D illustrates a scenario where a final resistance value of the fabricated Nwell termination resistor 150 results in an inadequate termination resistance. As illustrated by the timing diagram depicted in FIG. 2D, the pull-up signal PDRVG0 starts to pull the pad 160 high, as it is initially turned on, as depicted with reference to FIGS. 2A and 2B, while all of the pull-down devices are turned off.

However, once the PDRVG1 signal is turned on, output driver 100 will drive strongly due to the fact that the strongest pull-down leg is now turned on.

**[0028]** Representatively, once the strongest pull-down leg is activated by PDRVG1 signal 112 (FIG. 1), the slew rate of the driver output signal will exceed the predetermined slew rate range. A similar situation occurs during pull-down of the output buffer pad 160, such that once the stronger of the pull-down legs is turned on, the output signal slew rate will exceed the pre-determined range. In one embodiment, the pre-determined slew rate range is 0.4 v/ns to 1.0 v/ns. As described above, an extremely high slew rate, due to abnormally low Nwell termination resistance 150 can lead to problems, such as voltage reflections and interference in received or transmitted signals.

**[0029]** Conversely, as illustrated with reference to FIG. 2E, FIG. 2E illustrates a scenario where the final fabricated resistance value of the Nwell termination resistor 150 is at an excessive resistance value. As illustrated by the timing diagram of FIG. 2E, the driver output signal slew rate will transition at a rate which is below the pre-determined range as described above. As a result, the amount of time required for completion of the falling signal transition or rising signal transition will be slow, which can lead to problems in meeting timing specifications, such as set-up times of various devices that may be connected to the driver 100.

**[0030]** Referring now to FIG. 3, FIG. 3 depicts the conventional output driver as originally depicted in FIG. 1 to illustrate pull-down crowbar current 176 and pull-up crowbar current 174. As illustrated with reference to FIGS. 4A and 4B, during a rising signal transition, a smaller of the pull-down signals, such as for example NDRVGO, may stay on through all or a portion of the rising signal transition. When such a scenario occurs, a crowbar current is burned, as illustrated by crowbar current 174. Conversely, during a falling signal transition, a smaller of the pull-up legs may be left on during all or a portion of the falling signal transition to generate pull-down crowbar current 176.

**[0031]** Unfortunately, such crowbar currents will result in a reduced slew rate of the driver output signals due to the fact that the crowbar currents will either divert current

from the pad 160 during a rising signal transition or reduce the amount of current that is pulled from the pad 160 during a falling signal transition. Accordingly, the combination of variations in termination resistances, as well as crowbar currents, can lead to problems in meeting timing specifications. As a result required slew rate ranges often cannot be met by output drivers in conventional devices.

**[0032]** Referring now to FIGS. 5 and 6, FIGS. 5 and 6 depict output driver 400, which utilizes a pair of compensation resistive elements (450 and 460) to provide compensation for resistive variation of signal termination devices, which utilize an Nwell resistor 430. Accordingly, as illustrated, output driver 400 includes a pull-up circuit having a plurality of pull-up devices 410 (410-1, . . . , 410-N), which are activated by a pull-up pre-driver 470. In the embodiment depicted, the pull-up drivers are illustrated as metal-oxide-semiconductor (MOS) field-effect transistors (FETs) (MOSFET) device. In the embodiment depicted, the pull-up devices are illustrated as P-type MOS set devices, such that a negative or zero voltage level at a gate 414 of the pull-up devices turns on the devices.

**[0033]** Accordingly, as illustrated, the MOSFET devices are illustrated as switch level models. In one embodiment, output driver 400 further includes a pull-down circuit having a plurality of pull-down devices 420 (420-1, . . . , 420-N). In the embodiment illustrated, the pull-down devices are illustrated as N-type MOSFET devices, such that a positive voltage level at gate 424 turns on the devices. As such, the pull-down devices are activated by pull-down pre-driver 480, which generates pull-down signals (NDRVGN 422-N and NDRVGO 422-1).

**[0034]** As such, although output driver 400 is illustrated utilizing MOSFET devices to achieve rising and falling signal transitions, the embodiment depicted such not be construed in a limiting sense, as it is merely intended to provide an example of the embodiments described herein, whether than to provide an exhaustive list of all possible implementations of the embodiments described herein. In addition, in practice, output drivers may utilize any number of pull-down and pull-up devices. As such, the pair of pull-up and pull-down devices illustrated in FIGS. 5 and 6 are provided to avoid obscuring the details of the embodiments described herein.

**[0035]** Referring again to FIG. 5, and in contrast to the conventional driver 100 as depicted in FIG. 1, the output driver 400 makes use of crowbar current 490. As known to those skilled in the art, a crowbar current occurs when opposing legs, which are normally turned off to generate either a rising signal transition or falling signal transition remain active for all or a portion of the signal transition. Accordingly, when an opposing leg is left on, a current will flow through the opposing leg and provide contention with the rising or falling signal transition.

**[0036]** For example, as depicted in FIG. 5, FIG. 5 illustrates a rising signal transition in output driver 400, while FIG. 6 depicts a falling signal transition in output driver 400. Accordingly, during a rising signal transition, pull-down devices 420 will

generally be turned off and simultaneously, one or more of the pull-up devices 410 may be turned on. However, if, for example, a weak pull-down leg of the output driver, such as for example pull-down leg 420-1, is left on during a portion or all of the rising signal transition, a crowbar current 490 is generated, which flows from pull-up device 410 through pull-down device 420-1 and through ground 404.

**[0037]** However, during a rising signal transition, the pull-up devices are trying to provide current 492 to driver output pad 440 to raise the voltage level at output pad 440 to indicate a rising signal transition. Unfortunately, crowbar current 490 will, in effect, slow down the rising signal transition at the driver output pad 440 by diverting a portion of pull-up current 492 through pull-down leg 420-1. Generation of the crowbar current is further illustrated with reference FIGS. 7A and 7B.

**[0038]** As illustrated in FIG. 7A, FIG. 7A depicts analog compensation pull-up pre-drive signals 300, while FIG. 7B depicts analog compensation pull-down pre-drive signals 330. Accordingly, as illustrated by FIGS. 7A and 7B, while a conventional driver as depicted in FIG. 1 would de-activate pull-down legs simultaneously to begin a rising signal transition, a weaker of the pull-down legs, for example pull-down leg 420-1, is left on by delaying de-activation of the NDRVG0 signal 422-1. As such, until the NDRVG0 signal is deactivated in FIG. 7A, crowbar current 490 will flow through the weaker pull-down leg 420-1 as illustrated in FIG. 5.

**[0039]** In contrast, during a falling signal transition, instead of simultaneously deactivating the pull-up legs 410, a weaker of the pull-up legs, for example pull-up leg 410-1 is left on by delaying de-activation of the PDRVGG signal. As such, until the PDRVGG signal is deactivated in FIG. 7B, crowbar current 499 will flow from the driver supply voltage 402 through the stronger of the pull-down legs, such as for example pull-down leg 420-N as illustrated in FIG. 6.

**[0040]** Although crowbar current is generally considered an undesirable effect, utilizing of the embodiments described herein, the crowbar current 490/494 may be utilized to provide analog compensation of variations in the driver impedance due to utilizing, for example an Nwell resistor as signal termination device 430. As will be described in further detail below, driver 400 utilizes a pair of Nwell compensation resistive elements 450 and 460, which are coupled in series with the weaker of the pull-up and pull-down legs and connected to the signal termination device 430. As such, during fabrication of output driver 400, driver 400 may be simulated based on a selected resistance level of the signal termination device 430.

**[0041]** Based on the simulation, the compensation resistor levels may be selected to achieve an output driver slew rate, which is between 0.4 v/ns and 1.0 v/ns. As such, the slew rate refers to a slope of the rising or falling signal transition, which in one embodiment is between 0.4 v/ns and 1.0 v/ns. However, once the output driver is fabricated, the variation in the Nwell resistor material will either increase or decrease resistance of both the

compensation resistors 450 and 460, as well as the signal termination 430. As such, assuming for example that the termination device 430 achieves an excessive resistive level, the compensation resistors 450 and 460 will also achieve a final excessive resistive level.

**[0042]** Consequently, referring again to FIG. 5, assuming a rising signal transition, the rising signal transition is drastically slowed. In other words, the excessive resistive level of the termination device 430 will limit the amount of current which is provided to the pad 440 to raise the pad voltage level to indicate a rising signal transition. However, the crowbar current 490 will also be decreased by an equivalent proportion. Consequently, by decreasing the amount of crowbar current from the amount determined during the initial circuit simulation, output driver 400 will achieve an output driver slew rate that is within the desired slew rate of 0.4 v/ns and 1.0 v/ns.

**[0043]** In contrast, assuming the final fabricated resistive level of the termination resistor 430 is very low, the resistive level of the compensation resistive elements will also be very low. As described above, when the resistive level is too low, the current 492 flow into the driver output pad 440 will be at a very high level, which will cause the output pad voltage level to have an excessive slew rate. However, due to the fact that the compensation resistive elements 450 and 460 will be set to a very low resistance level, the compensation resistive elements 450 and 460 will allow an increased crowbar current 490/494, which will provide contention with the signal transition current 492/496 and slow down the slew rate of the driver output pad output signal. Consequently, the output pad output signal slew rate will remain within the predetermined range, as described above.

**[0044]** Referring now to FIG. 6, FIG. 6 illustrates a falling signal transition within output driver 400. As illustrated, the crowbar current 492 is generated by delaying deactivation of the weak pull-down leg 410-1 during a falling signal transmission. Assuming output driver 400 is fabricated with a resulting termination device resistance at an extremely high resistance value, the pull-down current 496 will be reduced in magnitude due to the high resistance level. However, the compensation resistive element 450 will also have a drastically increased resistive level, which increases proportionally to the termination resistive level. As such, the crowbar current 492 will be drastically reduced beyond the simulated crowbar current level. As a result, the decreased crowbar current 494 will compensate for the decreased pull-down current 496.

**[0045]** Consequently, the pull-down current 496 will be less effected by the presence of crowbar current, 494 resulting in an output signal slew rate, which is within the predetermined range. In contrast, if the Nwell resistive material is fabricated with a final resistance level which is too low, the pull-down current 496 will be increased by a dramatic amount. However, the crowbar current 494 will also be increased by the exact amount or a magnitude thereof and provide contention with the pull-down current 496. This signal contention will slow down the falling signal transition. As a result, the final slew rate of

the output signal at the driver output pad 440 is compensated to remain within the predetermined range.

**[0046]** Accordingly, as illustrated by FIG. 7C, the output driver signal slew rates will be compensated by either increased or decreased crowbar current, resulting in an output signal slew rate, which is within the predetermined range. Accordingly, output drivers utilizing the embodiments described herein are capable of interfacing with legacy devices, which use Nwell termination resistive elements. In addition, although FIGS. 5 and 6 are illustrated with resistors as the compensation resistive elements 450 and 460, those skilled in the art will appreciate that other types of resistive elements may be utilized, such as transistors or other resistive elements as known to those skilled in the art. Other such devices may be used as compensation elements, provided their resistance varies in correspondence with the primary termination device.

**[0047]** Referring now to FIG. 8, FIG. 8 depicts a block diagram illustrating a system chipset 500 utilizing output drivers 400, which implement compensation resistive elements to compensate the driver output signal slew rate against device impedance variation, in accordance with one embodiment. As described herein, the term “chipset” is used in a manner to collectively describe the various devices coupled to processor 502 to perform desired system functionality. Representatively, system chipset 500 includes processor 502 coupled to a host controller 510 via, for example a front side bus 504. Host controller 510 is coupled to memory 520 via, for example a memory bus. In one embodiment, output controller 530 is also coupled to host controller 510 via, for example a system bus 522.

**[0048]** The I/O controller 530 utilizes output drivers 400 to operate as I/O drivers including compensation resistive elements to maintain output signal slew rates within a predetermined range. In one embodiment, I/O driver 400 is coupled to a peripheral component interconnect (PCI) bus 550, which is coupled to one or more PCI slots 560 (560-1, . . . , 560-N). In one embodiment, the I/O controller 530 includes a plurality of output drivers 400 (400-1, . . . , 400-N) for coupling to one or more IDE or legacy devices 540 (540-1, . . . , 540-N). As a result, the I/O controller 530 can utilize output drivers which include on-chip signal termination provided via Nwell resistors. Consequently, Nwell resistors are selected for use as on-chip signal termination based on their lower cost, as well as requiring a minimal die area when fabricated.

**[0049]** Consequently, using compensation resistive elements as depicted in FIGS. 3 and 4 within I/O drivers 400, the I/O controller 500 can ensure that the output signal slew rate to communicate with either the PCI slots 560 or IDE devices 540 is within a predetermined range. In addition, when device impedance variations occur within the resistive elements of drivers 400, such as the signal termination device, the compensation resistive elements will provide analog compensation of the output driver signal slew rate

due to the fact that the variations between the signal termination device, as well as the compensation resistive elements, will be equal in magnitude.

**[0050]** Turning now to FIG. 9, what is shown is a block diagram of an embodiment of an electronic system 600 in which an I/O section utilizes compensation resistive elements as described above. The system has a multilayer printed wiring board 604 on which a parallel bus 608 is formed. The bus 608 may be of the point-to-point variety, or multi-drop buses, such as those used in a main memory. An integrated circuit (IC) chip packet 606 is operatively installed on the board to communicate using the parallel bus 608.

**[0051]** In one embodiment, installation of the package 606 may be done by a surface mount technique or via a connector or socket. The package includes an IC chip (chipset) 610 that includes a logic function section and an I/O section (driver/receiver) as an interface between the logic function section and the bus 608. The logic function may be one of the following well-known devices: a microprocessor, a memory controller, an I/O controller hub, an integrated driver electronics (IDE) output driver, or the like. Alternatively, other devices that can be implemented in the logic function section of an IC chip may be used.

**[0052]** In the embodiment described, the I/O section includes a chipset driver which utilizes a pull-up compensation resistive element and a pull-down compensation resistive element, which are set to provide resistive analog compensation of driver output slew rate against impedance variation. A second IC chip package 612 is also installed on the board 604 to communicate with the first package 606 via the bus 608. The second IC package 712 also includes a chip 614 having an I/O section in which a chipset receiver is provided to interface the bus 608 and its own function logic section (here shown as a device plug-in card).

**[0053]** According to an embodiment, the I/O interfaces of the two chips 610 and 612 may communicate with each other bi-directionally, that is using the same conductive lines of the bus for both transmitting and receiving data. Thus, in such an embodiment, drivers are provided in both IC chips that are connected to the same conductive lines of the bus 608. Other system applications of the compensation resistance are possible, including for example, virtually any chipset driver which is limited by variations of device impedance which cause slow rate variations which signals must propagate and reach a destination at a desired signal level. Procedural methods for implementing circuit design automation of the I/O driver claimed by the embodiments described herein are now described.

#### Alternate Embodiments

**[0054]** Several aspects of one implementation of the output driver for providing analog compensation of driver output slew rate against device impedance variation have been described. However, various implementations of the pull-up and pull-down compensation resistive elements provide numerous features including, complementing,

supplementing, and/or replacing the features described above. Features can be implemented as part of the I/O driver or as part of a controller hub in different implementations. In addition, the foregoing description, for purposes of explanation, used specific nomenclature to provide a thorough understanding of the embodiments described herein. However, it will be apparent to one skilled in the art that the specific details are not required to practice the embodiments described herein.

**[0055]** In addition, although an embodiment described herein is directed to an I/O driver, it will be appreciated by those skilled in the art that the embodiments described herein can be applied to other systems. In fact, systems for utilizing on-chip signal termination are within the embodiments described herein, without departing from the scope and spirit of the embodiments described herein. The embodiments described above were chosen and described to best explain principles and its practical applications. These embodiment were chosen to thereby enable others skilled in the art to best utilize the various embodiments with various modifications as are suited to the particular use contemplated.

**[0056]** It is to be understood that even though numerous characteristics and advantages of various embodiments have been set forth in the foregoing description, together with details of the structure and function of various embodiments, this disclosure is illustrative only. In some cases, certain subassemblies are only described in detail with one such embodiment. Nevertheless, it is recognized and intended that such subassemblies may be used in other embodiments. Changes may be made in detail, especially matters of structure and management of parts within the principles of the embodiments described herein to the full extent indicated by the broad general meaning of the terms in which the appended claims are expressed.

**[0057]** The embodiments described herein provide many advantages over known techniques. The embodiments described herein include the ability to provide a true analog compensation for the effects of termination resistance on the output driver slew rate, while not requiring any additional pins. The embodiments make use of an already present feature of output drivers (crowbar current), which is often considered undesirable to produce effective slew rate compensation. Crowbar current is frequently used to control signal edge rates, but it has not been used to compensate for on-chip termination resistance variations before now.

**[0058]** Furthermore, the simplicity of one embodiment is unmatched by other compensation schemes. No additional circuitry is required other than the compensation resistors themselves. Moreover, the output driver signal must be tuned to control the duration that the crowbar current flows, but this does not add requirements beyond what is needed for normal output driver control. Furthermore, manufacturing costs are saved by allowing the use of cheaper resistive elements to be used for on-chip signal termination. As a result, any manufacturer of integrated circuits containing on-die termination devices for high speed chip signaling could benefit from the embodiments described herein.

**[0059]** Having disclosed exemplary embodiments, modifications and variations may be made to the disclosed embodiments while remaining within the scope of the embodiments described herein, as defined by the following claims.